ABSTRACT

The SRAM cells of a semiconductor storage device each comprise first and second inverter circuits loop-connected with each other to form a hold circuit; two access transistors; and a hold control transistor connected in series with a drive transistor of the second inverter circuit. While the memory cell is not accessed, the hold control transistor causes the first and second inverter circuits to form the loop connected hold circuit for statically holding data. When the memory cell is accessed, the hold control transistor causes the first and second inverter circuits to be disconnected from the loop connection for dynamically holding data, thereby preventing data corruption that would otherwise possible occur due to a read operation. Moreover, a sense amplifier circuit that uses a single bit line to read data from a memory cell is disposed in a space appearing in the memory cell array, thereby effectively using the area.